

## Advanced Forward Error Correction Systems Using H.Code<sup>1</sup> Algorithms

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Technology Enhancement Partners, LLC, (also known as TEPartners) has developed a new approach to building Forward Error Correction, FEC, Systems. The TEPartners' approach, using the patent pending H.Code algorithms, produces units with a paradigm shift in Error Detection and Correction technology. With the H.Code algorithms, VHDL design technology and FPGA IC implementation, TEPartners has achieved significant improvements in burst and random bit error correction over the norm in FEC implementation. TEPartners' units use single IC implementations for both the Encoder and Decoder – Corrector units resulting in a significant reduction in size, weight, power consumption, and cost. The H.Code algorithms permit TEPartners to use parallel processing throughout their designs and obtain high throughput with low processing latency. The units produced have a high level of error correction capability at the very lowest communication overhead for all manners of digital communication.

The most unique feature of the H.Code algorithms is that they can be arranged to optimize the FEC system to achieve the best performance characteristics for the intended application. Originally, a demonstration version was developed to illustrate H.Code performance at eliminating SEU induced RAM bit errors and IC failure induced eight bit or more block errors. Very small programmable gate arrays were used for the implementation and the EDAC operations added only a few nanoseconds to the minimum cycle time. The design was extended to show that building a fully fault tolerant memory system is fully practical and considerably less costly than using a triple redundant implementation approach.

A version of the H.Code has also been proposed for use as an alternate Secure Hash Algorithm to provide multiple modification detection and correction. Total software processing of the H.Code algorithms is practical. The produced signature can easily be less than 1% the size of the data file being signed. Multiple H.Code algorithms can be used in each system to produce industry standard signatures for wide distribution communication, system standard signatures for limiting distribution to a particular site, and processor unique signatures for maximum-security purposes.

Most recently, under a US Government contract TEPartners designed and built a demonstration system that uses a 32-bit data block for an overhead of 6.25%. For this implementation the input data rate was 115,200 bps over an RS-232C channel. The input data was received in bursts and processed in bursts and was transmitted continuously over a voice grade communication channel at a 64 Kbps data rate (see Figure 1). The FEC system employs an encoding arrangement to demonstrate both one and two dimensional error correction. The coding interleaved three code vectors for correction of random bit errors and bursts of errors, up to sixty-seven bits long. With the first dimensional processing a correction performance of improving a  $10^{-4}$  average bit-error rate to a  $10^{-14}$  average bit-error rate was achieved. Then, together with the second dimensional processing, the system achieved an improved performance by correcting error bursts up to seven thousand bits long and improving a

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<sup>1</sup> H.Code is a trademark of Technology Enhancement Partners, LLC of Medford Lakes, New Jersey.

$10^{-3}$  bit-error rate to a  $10^{-14}$  bit-error rate. This would be attractive for its ability to remove errors from data communication.

The latency for the first dimension processing, due to the 64 Kbps data rate of the channel, was slightly less than 0.21 seconds for both encoding and error correction. The latency for the second dimension processing, also due to the 64K bps data rate of the channel, was slightly less than 5 seconds. For the Demonstration System the Encoder Unit and Decoder – Corrector Units are packaged in separate 208-pin TQFP FPGAs with a single 32-pin dual-in-line SRAM used with the Decoder – Corrector Unit. The FPGA cell usage for these two units is given in Table 1.

**Table 1: FEC FPGA Design and Layout Results**

		Chip Cells	Chip Cells	Chip I/Os	Chip PLLs
Actel Chip	FEC Design	Core	RAM/FIFO	Usage	Usage
APA 300	Encoder	2668/32.6%	32/100%	37/23.7%	0/0%
	Decoder – Corrector	3112/38.0%	20/62.5%	61/39.1%	0/0%

This FEC version was developed to demonstrate the performance that could be achieved for a covert UAV application. In this application the sensor would be a miniature camera with video compression on-board processing followed by an FEC Encoder Unit whose output would be fed to a transmitter that would continuously send RS-232C signals over a 64Kbps channel to a remote ground station. The UAV would not have an uplink downlink for command, control or resynchronization. To get around any loss of synchronization TEPartners developed a unique approach for sending a sync pattern at the appropriate times at the cost of less than a 1% increase in the communication overhead.

To improve the data recovery performance the FEC Units would use a TEPartners developed unique two-dimensional encoding for error detection and correction processing. Because H.Code error correction can use the redundant information to correct errors in the received data and can use the data to correct errors in the received redundant information, the Decoder – Corrector unit processes the received data to first perform the correction of both the data and the redundant information in one of the dimensions. That “first dimension corrected” data and redundant information is then provided to the second dimension of processing to perform further correction of both data and redundant information as well as being made available as a Decoder – Corrector output, in an RS-232C format, for display. After processing the data and redundant information in both dimensions the “two dimension corrected” data and redundant information is made available as a Decoder – Corrector output, in an RS-232C format, for display and/or used as the input to another Decoder – Corrector unit for further processing. At the cost of a higher processing latency, this two dimension processing approach vastly increases the amount of the original information recovered from the corrupted received information.

For subsequent implementations TEPartners will use revised architectures and data encoding approaches in which the RAM IC will not be needed. TEPartners is presently developing an FEC that uses a multi level encoding and processing arrangement that will substantially improve the FEC system’s multiple burst error and bit error correction capability while eliminating the large second dimension processing latency and the external Decoder – Corrector RAM required for the two dimensional processing system developed for the autonomous UAV application. This new architecture for the FEC system units will incorporate parallel input and output channels to produce a top data

throughput in excess of a Gbps with a processing latency of less than a millisecond. This class of FEC systems is targeted for application in wide-band data communication links of either the broadcast or hard line variety.

All FEC systems built by TEPartners using the new architecture can be customized to provide optimum performance for the application. Using H.Code, there will be no data tables used as parts of the encode and decode processes and each FEC system design will be based on different data block sizes for specific operating conditions. Further, if the customer desire, the system will be based on unique versions of the H.Code equations. Thus, the operation of each system can be matched to best handle the type of channel over which the data is to be transmitted and the error patterns that are expected. Multiple solutions can be put into a single implementation because the implementation cost, size, weight and power consumption of an H.Code FEC system are small and the maximum operating speed can be made high enough to handle a wide range of applications.

Only TEPartners' H.Code FEC systems can provide these features for digital data communication.

**Figure 1: The Demonstration FEC System**

